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Power saving system.

Abstract:

In a personal computer having a logic circuit constituted by low-power consumption elements such as CMOS elements, a power saving system includes a register (41) in which control data can be set from a keyboard (29) or by software, and switches (43) for allowing and stopping power supply from a power-supply to an oscillator on the basis of control data from the register. Supply of clock signals to a disabled logic circuit can be stopped by an operator's decision. In initialization processing of a driver routine of an extended card optionally connected to the personal computer, power supply designation information is set in the register. In the completion routine, power supply stop designation information is set in the register.

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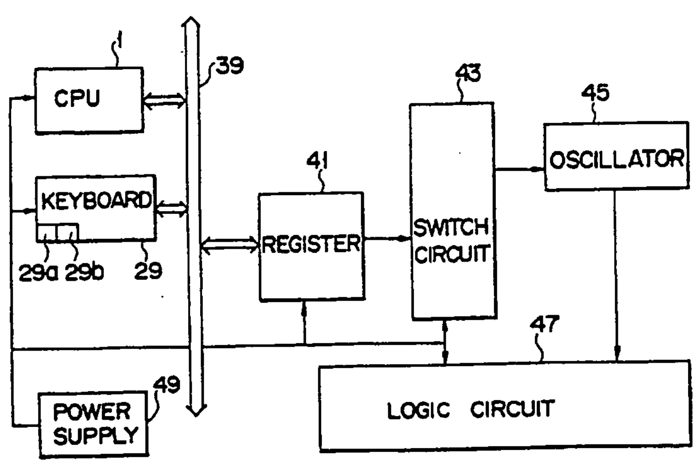
(54) Power saving system.

(57) In a personal computer having a logic circuit constituted by low-power consumption elements such as CMOS elements, a power saving system includes a register (41) in which control data can be set from a keyboard (29) or by software, and switches (43) for allowing and stopping power supply from a power supply to an oscillator on the basis of control data from the register. Supply of clock signals to a disabled logic circuit can be stopped by an operator's decision. In initialization processing of a driver routine of an extended card optionally connected to the personal computer, power supply designation information is set in the register. In the completion routine, power supply stop designation information is set in the register.



F I G. 2

EP 0 381 021 A2

Power saving system

The present invention relates to a power saving system having a logic circuit constituted by CMOS (Complementary Metal Oxide Semiconductor) elements and applied to, e.g., a personal computer.

In recent years, various types of chips such as microprocessor, memory and LSI chips are manufactured along with developments in semiconductor technologies, and packing densities of these chips are increasing year by year. As a result, compact personal computers have been developed, and for example, compact, light-weight, portable personal computers called lap-top computers have been very popular in place of desk-top personal computers. Most of the lap-top computers are designed as battery-operated computers. For this reason, these computers are designed to minimize power consumption of the internal circuits in order to prolong the operating time.

It is known that power consumption of a CMOS is minimized when a clock pulse is not supplied. A power-saving implementation is proposed wherein LSIs (Large Scale Integration Circuits) used in internal circuits of computers are arranged by CMOS elements.

Wasteful power consumption such as power consumption required for waiting for a key input from a keyboard is still present. Strong demand has arisen for further power saving.

It is an object of the present invention to provide a power saving system which utilizes CMOS characteristics which exhibit minimum power consumption in the absence of input clock pulses, thereby performing power saving in accordance with a software instruction.

According to the first aspect of the present invention, a power saving system for a personal computer which includes a logic circuit constituted by highly integrated semiconductor elements, comprises: a power supply for supplying power; clock signal generating means for receiving the power from the power supply and supplying a clock signal to the logic circuit; keyboard means including at least a power supply designation key for designating power supply to the clock signal generating means and a power supply stop designation key for designating stop of power supply to the clock signal generating means, and for outputting power supply designation information and power supply stop designation information; latch means for latching the power supply designation information or the power supply stop designation information from the keyboard means; and switch means, connected between the latch means and the clock signal generating means, for supplying the power to the clock signal generating means on the basis of the power supply designation information supplied from the latch means and for stopping power supply to the clock signal generating means on the basis of the power supply stop designation information supplied from the latch means.

According to the second aspect of the present invention, a power saving system for a personal computer which includes a logic circuit constituted by highly integrated semiconductor elements and receives an input signal and outputs a predetermined signal, comprises: a power supply for supplying power; clock signal generating means for receiving the power from the power supply and supplying a clock signal to the logic circuit; latch means for latching power supply stop designation information; memory means for storing a control program serving as a logic circuit driver routine executed by the personal computer, the control program determining whether a predetermined signal is output from the logic circuit within a predetermined period of time and setting the power supply stop designation information in the latch means when the predetermined signal is not output within the predetermined period of time; and switch means, connected between the latch means and the clock signal generating means, for stopping power supply to the clock signal generating means on the basis of the power supply stop designation information supplied from the latch means.

According to the third aspect of the present invention, a power saving system for a personal computer, comprises: a power supply for supplying power; extended card means, optionally connectable to the personal computer, for executing a predetermined logical function; clock signal generating means for receiving the power from the power supply and supplying a clock signal to the extended card means; latch means for latching power supply designation information or power supply stop designation information; memory means for storing a program serving as an extended card driver routine executed by the personal computer, the program including an initialization routine for setting the power supply designation information in the latch means and a completion routine for setting the power supply stop designation information in the latch means after a predetermined function is executed by the extended card means; and switch means, connected between the latch means and the clock signal generating means, for supplying the power to the clock signal generating means on the basis of the power supply designation information supplied from the latch means and for stopping power supply to the clock signal generating means on the

basis of the power supply stop designation information supplied from the latch means.

Additional objects and advantages of the invention will be set forth in the description which follows, and in part will be obvious from the description, or may be learned by practice of the invention. The objects and advantages of the invention may be realized and obtained by means of the instrumentalities and combinations particularly pointed out in the appended claims.

Other objects and features of the present invention will be apparent from the following description taken in connection with the accompanying drawings, in which:

Fig. 1 is a block diagram showing an arrangement of a personal computer which employs a power saving system according the present invention;

Fig. 2 is a block diagram of a power saving system according to the first embodiment of the present invention;

Fig. 3 is a data format showing bit assignment of a register shown in Fig. 2;

Fig. 4 is a flow chart for controlling power supply upon operations of power ON and OFF keys arranged on a keyboard;

Fig. 5 is a flow chart for controlling power supply by time-out;

Fig. 6 is a flow chart in which power supply control is utilized in a driver routine of an extended card optionally connected to the power saving system; and

Fig. 7 is a block diagram showing a power saving system according to the second embodiment of the present invention.

Fig. 1 is a block diagram showing an arrangement of a personal computer which employs a power saving system according to the present invention.

Referring to Fig. 1, a CPU (Central Processing Unit) 1 controls the overall system operations of the personal computer. A ROM (Read Only Memory) 3 stores a basic input and output operating system (BIOS) program for controlling inputs/outputs of the personal computer. This BIOS includes programs represented by flow charts of Figs. 4 to 6. A RAM (Random Access Memory) 5 stores application programs executed by this personal computer and various data. A DMAC (Direct Memory Access Controller) 7 comprises a commercially available LSI for controlling DMA. A PIC (Interrupt Controller) 9 comprises a commercially available LSI for controlling various circuit interrupts. A PIT (timer) 11 measures time. An RTC (Real Time Clock) 13 comprises a commercially available LSI for storing date, time, an the like.

An HDC (Hard Disk Controller) 15 comprises a commercially available LSI for controlling an HDD (Hard Disk Driver) 17. The HDD (Hard Disk Drive) 17 serves as an external storage unit for storing programs and data. An FDC (Floppy Disk Controller) 19 comprises a commercially available LSI for controlling an FDD (Floppy Disk Drive) 21. The FDD 21 serves as an external storage unit for storing programs and data as in the HDD 17. A PRTCONT (Printer Controller) 23 controls a printer. An SIO (Serial Input and Output Control Circuit) 25 comprises a commercially available LSI for controlling communication. A KBC (Keyboard Controller) 27 comprises a commercially available LSI for controlling a keyboard 29. The keyboard 29 comprises various keys for inputting various data and includes a power ON command key 29a for designating power supply and a power OFF command key 29b for designating power of power supply. A PDPC (Plasma Display Controller) 31 controls a PDP (Plasma Display) 33. A VRAM (Video RAM) 35 serves as a memory for storing the content displayed on the PDP 33. Data is read out from a kanji ROM 37 to display kanji characters, and the readout kanji information is displayed on the PDP 33. The CPU 1, the ROM 3, the RAM 5, the DMAC 7, the PIC 9, the PIT 11, the RTC 13, the HDC 15, the FDC 19, the PRTC 23, the SIO 25, the KBC 27, the PDPC 31, the VRAM 35, and the kanji ROM 37 are connected to a system bus 39.

Fig. 2 is a block diagram showing a power saving system according to the first embodiment of the present invention.

A register 41 is connected to the system bus 39. The register 41 stores control data for ON/OFF-controlling the power supply. More specifically, the register 41 comprises, e.g., a 16-bit register. As shown in Fig. 3, bit information for controlling power ON/OFF is assigned to, e.g., bit 0. That is, when bit 0 is set at logic "1", the power is supplied to the respective circuits. However, when bit 0 is set at logic "0", the power OFF state is set. A bit output from the register 41 is supplied to a switch circuit 43. This register 41 may be assigned to the RAM 5 in the form of, e.g., a memory mapped I/O. Alternatively, I/O device addresses may be assigned to this register. In either case, the register 41 can be accessed by software.

The switch circuit 43 comprises an electronic switch (constituted by, e.g., transistors) or a relay circuit. When a bit output from the register 41 is set at logic "1", the power is supplied from a power supply 49 to an oscillator 45. However, when the bit output is set at logic "0", the power supply is stopped. When the oscillator 45 receives the power through the switch circuit 43, the oscillator 45 outputs a clock signal to a logic circuit 7. The power supply 49 is connected to supply the power to the CPU 1, the keyboard 29, the register 41, the switch circuit 43, and the logic circuit 47. The logic

circuit 47 comprises a CMOS circuit for performing a predetermined function. For example, in the block diagram of Fig. 1, the logic circuit 47 corresponds to the DMAC 7, the PIC 9, the PIT 11, the RTC 13, the FDC 19, the PRTC 23, the SIO 25, the KBC27, the PDC 31, and the like. Although not illustrated, the logic circuit 47 also includes a LAN (Local Area Network) controller and a MODEM (Modulator Demodulator).

Power supply or stop of power supply can be designated automatically or by an operator. The flow chart shown in Fig. 4 exemplifies an operation for detecting depression of the power OFF or ON command key 29a or 29b arranged on the keyboard 29 and for allowing or stopping power supply from the power supply to the oscillator 45.

The CPU 1 determines in step 51 whether a key input is detected. If YES in step 51, the CPU 1 determines in step 53 whether the depressed key is the power OFF command key 29a. If YES in step 53, data "01" (hex) is set in the register 41 in step 55. As a result, bit data of "1" is supplied from the register 41 to the switch circuit 43, and then the switch circuit 43 supplies the power from the power supply 49 to the oscillator 45. Therefore, the oscillator 45 supplies a clock signal to the logic circuit 47, and the logic circuit is operated.

When the CPU 1 determines in step 57 that the power ON command key 29b is depressed, the CPU 1 sets data "00" (hex) in the register 41 in step 59.

Bit data of "0" is supplied from the register 41 to the switch circuit 43, and the switch circuit 43 does not supply the power to the oscillator 45. In this case, no clock signal is supplied from the oscillator 45 to the logic circuit 47. The power consumption of the logic circuit 47 becomes minimum, and the power can be saved.

Fig. 5 is a flow chart showing an operation for automatically controlling power supply to the KBC (Keyboard Controller) 27.

The CPU 1 determines in step 61 whether a key input is detected. If NO in step 61, a time-measuring software counter is incremented in step 63. The CPU 1 then determines in step 65 whether a predetermined period of time has elapsed. If NO in step 65, the CPU 1 repeats the operations in steps 61, 63, and 65. When the CPU 1 determines in step 65 that the predetermined period of time has elapsed, the CPU 1 sets data "00" (hex) in the register 41 in step 67. As described above, in this case, the switch circuit 43 does not supply the power to the oscillator 45, and the oscillator 45 does not supply the clock signal to the logic circuit 47 accordingly. As a result, the power consumption of the logic circuit 47 becomes minimum, and the power can be saved.

Fig. 6 is a flow chart showing an operation for automatically controlling power supply or stop of power supply when, e.g., a LAN drive routine is loaded or unloaded.

Assume that the system bus of the personal computer shown in Fig. 1 is connected to an external connector (not shown), and that a LAN control card serving as an extended card can be optionally connected to this personal computer. In this case, the LAN driver routine is prestored in the HDD 17. In order to perform LAN control, the LAN driver routine stored in the HDD 17 is loaded in the RAM 5 and is executed by the CPU 1.

In step 71 as an initialization routine, the CPU 1 sets data "01" (hex) in the register 41. The switch circuit 43 supplies the power to the oscillator 45, and the oscillator 45 then supplies a clock signal to the logic circuit 47 (in this case, to the LAN card). The LAN card is then operated. After the predetermined LAN processing routine is executed, the CPU 1 performs completion processing in step 73. In this completion processing, the CPU 1 sets data "00" (hex) in the register 41. In this case, the switch circuit 43 stops supplying the power to the oscillator 45. Therefore, the power consumption of the LAN card becomes minimum, and the power can be saved.

Fig. 7 is a block diagram of a power saving system according to the second embodiment of the present invention. The same reference numerals as in Fig. 1 denote the same parts in Fig. 2, and a detailed description thereof will be omitted.

In the embodiment shown in Fig. 7, power from a power supply 49 is always supplied to an oscillator 45. A clock signal is supplied from the oscillator 45 to a gate circuit 75. The gate circuit 75 comprises, e.g., an AND gate and supplies a clock signal from the oscillator 45 to a logic circuit 47 in response to an enable signal from a CPU 1. The enable signal supplied from the CPU 1 may be supplied from a keyboard as in Fig. 2 or may be obtained by utilizing the concept of time-out, as shown in Fig. 4, or an enable or disable signal may be formed in the initialization and completion routines in the extended load module, as shown in Fig. 6. The same effect as in the embodiment of Fig. 2 can be obtained in the above modifications.

In the second embodiment, the LAN card is exemplified as the extended card. However, the present invention is not limited to this. For example, power supply of various external optional cards, such as an SCSI (Small Computer System Interface) control card, various communication boards, a keyboard controller, a printer controller, a display circuit controller, and a modem card can be controlled.

In the above embodiment, the programs shown in Figs. 4 to 6 are stored in the ROM 3. However, these programs may be stored in, e.g., the HDD 17

and the FDD 21.

Additional advantages and modifications will readily occur to those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details, representative devices, and illustrated examples shown and described. Accordingly, departures may be made from such details without departing from the spirit or scope of the general inventive concept as defined by the appended claims and their equivalents.

Claims

1. A power saving system for a personal computer having a logic circuit (47) constituted by highly integrated semiconductor elements, a power supply (49) for supplying power, and an oscillator (45) for receiving the power from said power supply and supplying a clock signal to said logic circuit, characterized by comprising:
means (29a, 29b, Figs. 4, 5, and 6) for designating supply and stop of supply of the clock signal to said logic circuit; and
control means (41, 43, 75) for controlling the supply or the stop of supply of the clock signal to said logic circuit in response to designation information from said designating means.

2. A system according to claim 1, characterized in that said designating means comprises a keyboard (29) including at least a power supply designation key (29a) for designating power supply from said power supply to said oscillator and a power supply stop key (29b) for designating stop of power supply from said power supply to said oscillator, said keyboard (29) being arranged to output power supply designation information and power supply stop designation information.

3. A system according to claim 1, characterized in that said logic circuit receives an input signal and outputs a predetermined signal, and
said designating means comprises memory means (3, 17, 21) for storing a control program serving as a logic circuit driver routine executed by said personal computer, the control program setting the power supply stop designation information when the predetermined signal is not output from said logic circuit within a predetermined period of time.

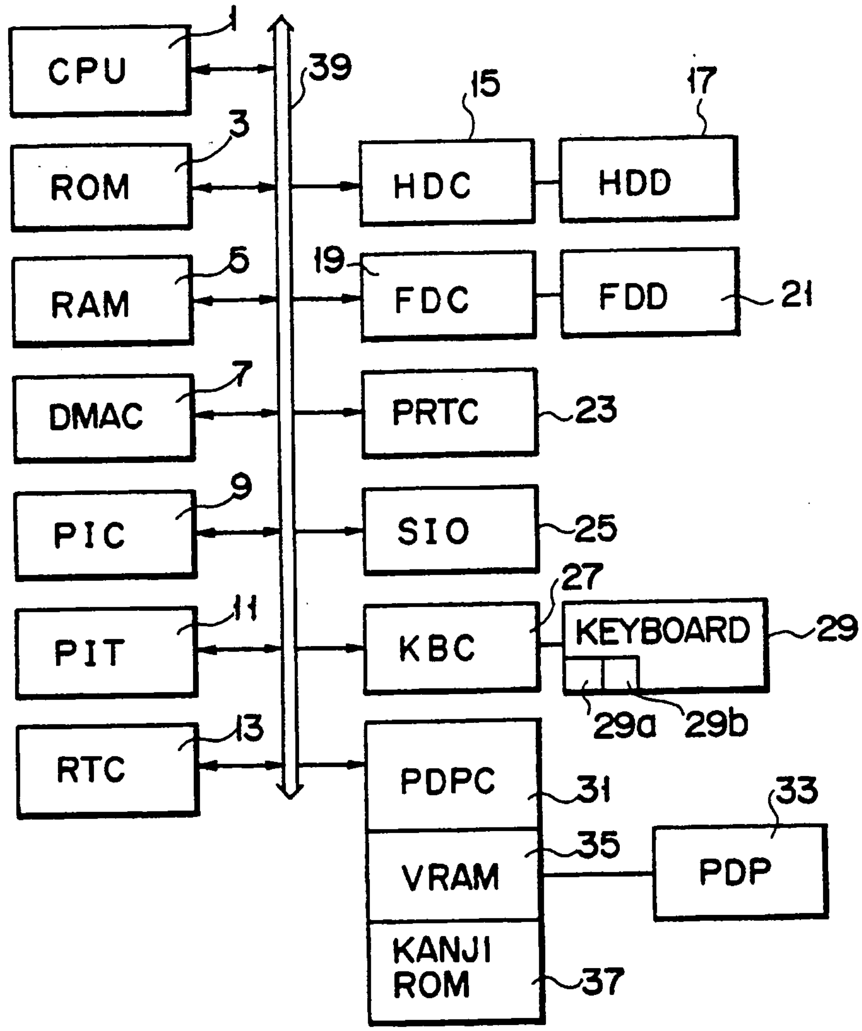
4. A system according to claim 1, characterized in that said logic circuit includes optional extended card means, connectable to said personal computer, for executing a predetermined logic function, and said designating means comprises memory means for storing a program serving as an extended card driver routine executed by said personal computer, the control program including an initialization routine for outputting power supply designation information and a completion routine for outputting the power supply stop designation information after the predetermined function is performed by said extended card means.

5. A system according to any one of claims 1 to 4, characterized in that said control means comprises:
latch means (41) for latching information for designating supply and stop of supply of the clock signal; and
switch means (43), connected between said latch means and said oscillator, for supplying the power to said oscillator on the basis of the clock supply designation information supplied from said latch circuit and for stopping power supply to said oscillator on the basis of the clock supply stop designation information supplied from said latch circuit.

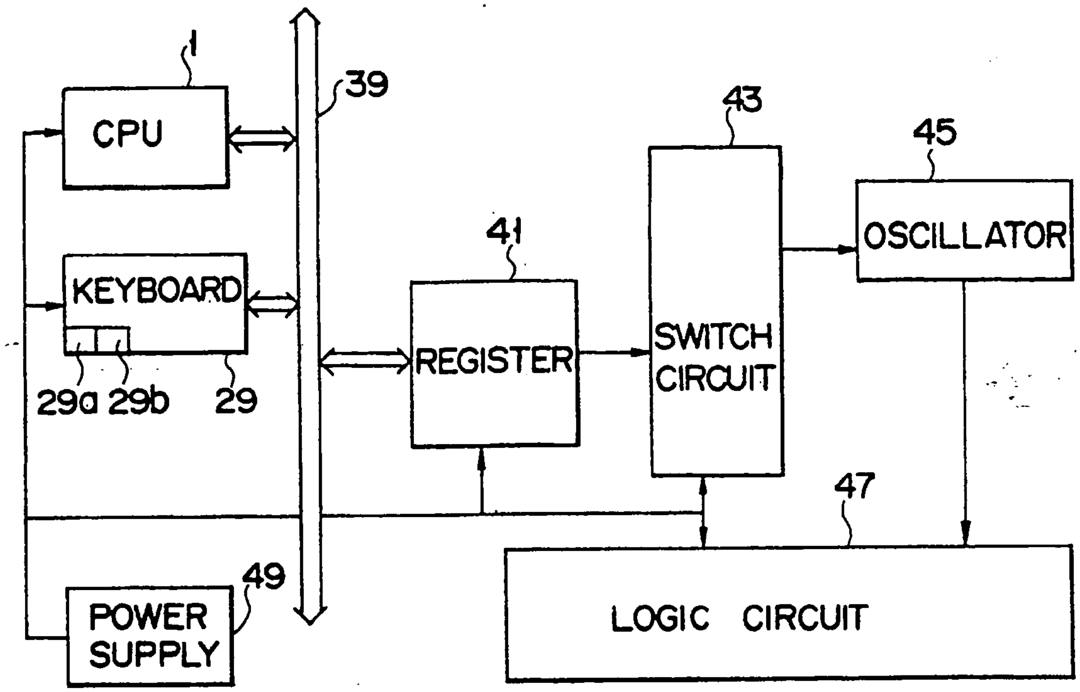
6. A system according to any one of claims 1 to 4, characterized in that said control means comprises gate means (75), connected between said oscillator and said logic circuit, for receiving the clock supply designation information and supplying the clock signal from said oscillator to said logic circuit, and for stopping supply of the clock signal to said logic circuit on the basis of the clock supply stop designation information.

7. A system according to any one of claims 1 to 6, characterized in that said logic circuit comprises CMOS (Complementary Metal Oxide Semiconductor) elements.

8. A system according to any one of claims 1 to 7, characterized in that said logic circuit includes a LAN (Local Area Network) control circuit, an SCSI (Small Computer System Interface) control circuit, a communication board, a keyboard controller, a printer controller, a display controller, and a model control circuit.

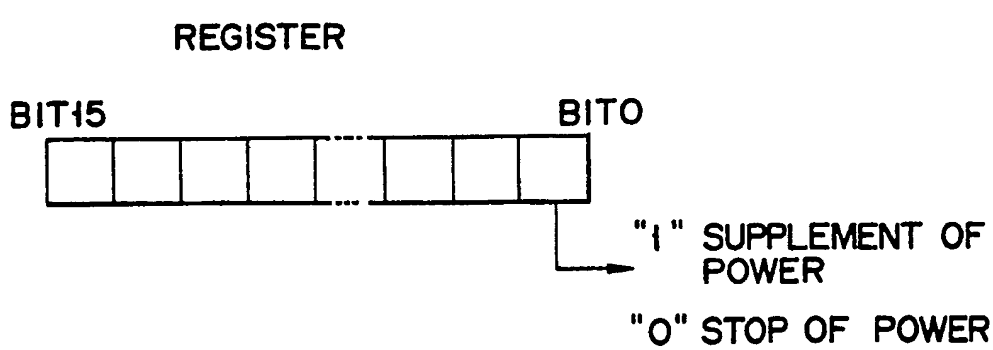

CPU
1
39
ROM
3
HDC
15
HDD
17
RAM
5
19
FDC
FDD
21
DMAC
7
PRTC
23
PIC
9
SIO
25
PIT
11
KBC
27
KEYBOARD
29
29a
29b
RTC
13
PDPC
31
VRAM
35
PDP
33
KANJI ROM
37

F I G. 1



CPU
1
39
KEYBOARD
29a 29b 29
REGISTER
41
SWITCH CIRCUIT
43
OSCILLATOR
45
47
LOGIC CIRCUIT
POWER SUPPLY
49

F I G. 2



REGISTER
BIT15
BIT0
"1" SUPPLEMENT OF POWER
"0" STOP OF POWER

F I G. 3

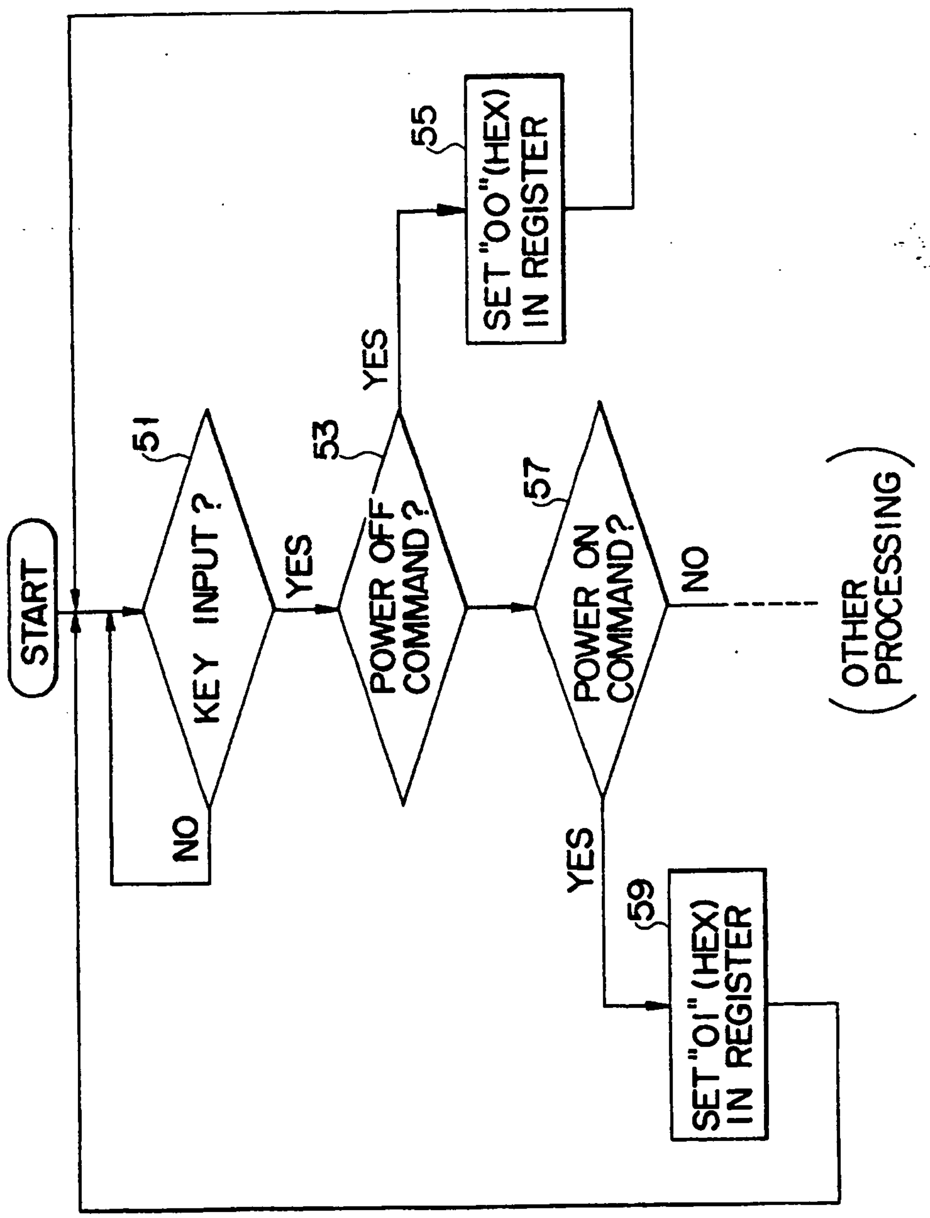
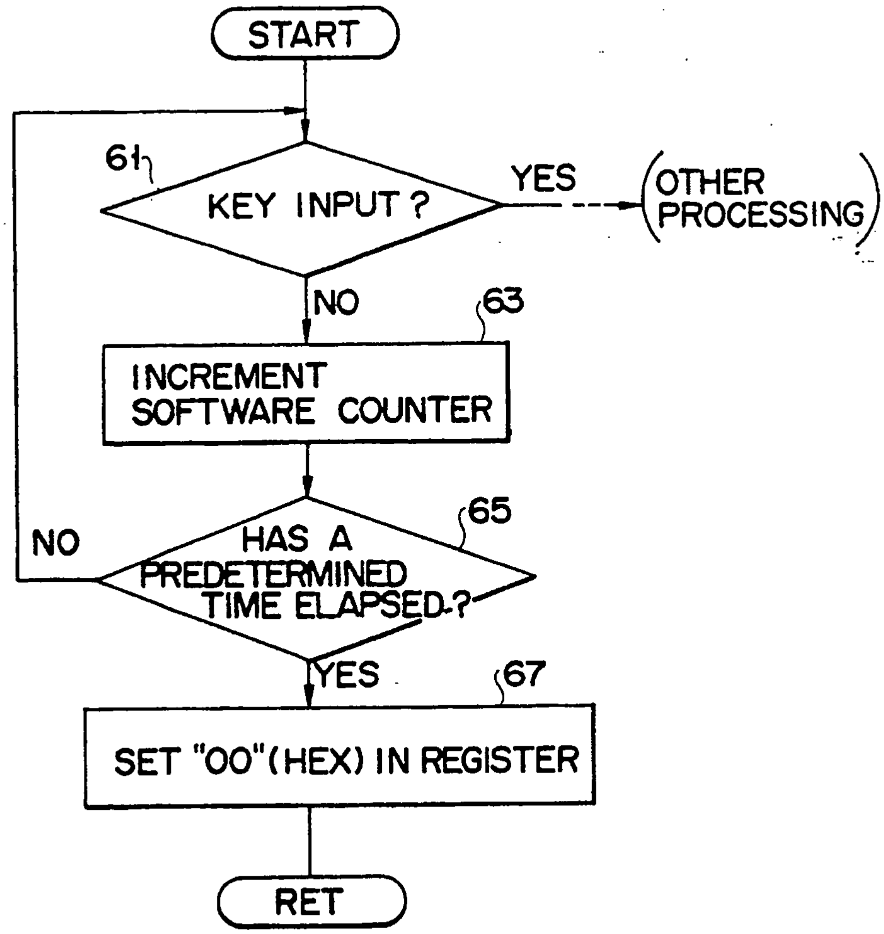
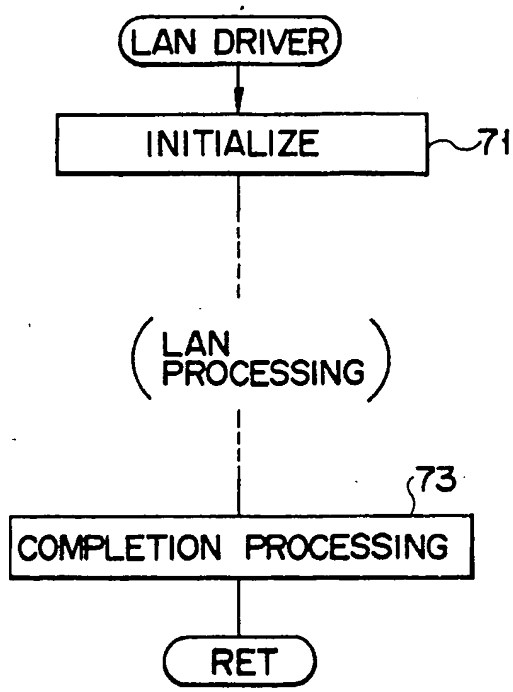

START
51
KEY INPUT ?
NO
YES
53
POWER OFF COMMAND ?
YES
55
SET "OO" (HEX) IN REGISTER
57
POWER ON COMMAND?
NO
(OTHER PROCESSING)
YES
59
SET "OI" (HEX) IN REGISTER

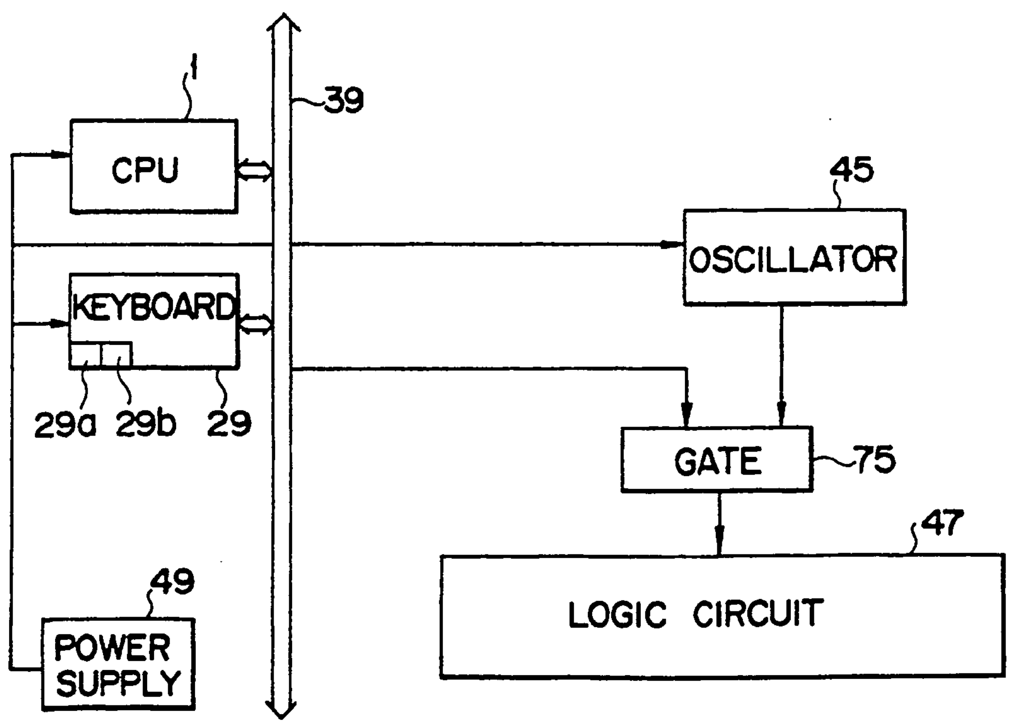
FIG. 4


START
61
KEY INPUT ?
YES
OTHER PROCESSING
NO
63
INCREMENT SOFTWARE COUNTER
65
NO
HAS A PREDETERMINED TIME ELAPSED ?
YES
67
SET "OO"(HEX) IN REGISTER
RET

F I G. 5


LAN DRIVER
INITIALIZE
71
LAN PROCESSING
73
COMPLETION PROCESSING
RET

F I G. 6


1
39
CPU
45
OSCILLATOR
KEYBOARD
29a 29b 29
GATE
75
47
LOGIC CIRCUIT
49
POWER SUPPLY

F I G. 7